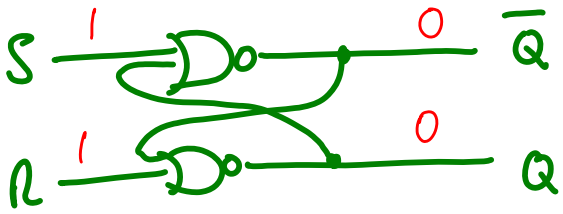
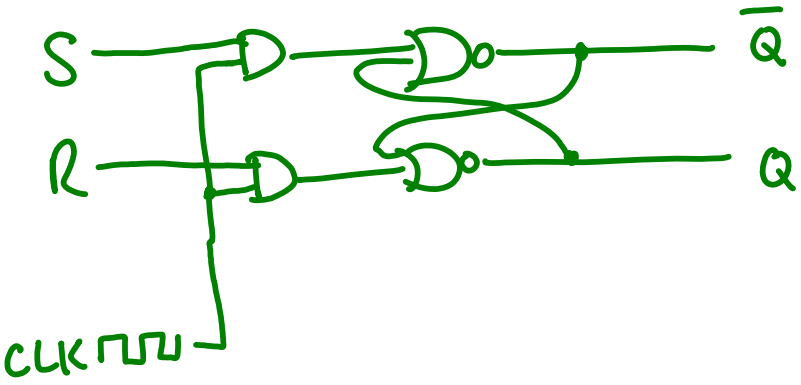
Instability of SR flip-flop

It's easy to see that when $S = R = 1$, both Q and $\overline{Q}$ are forced to zero:

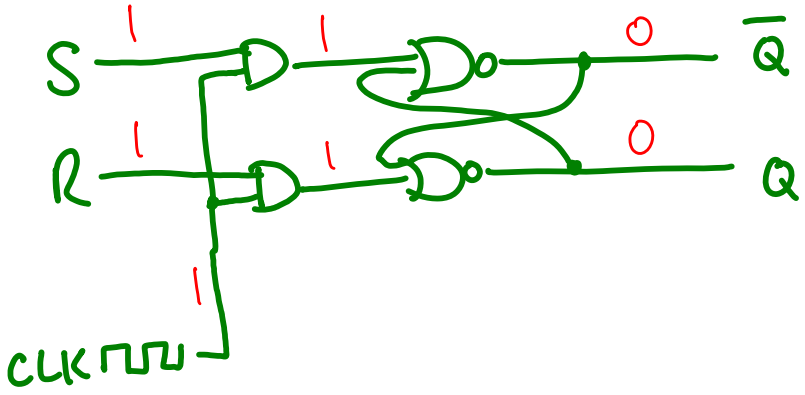


(A)

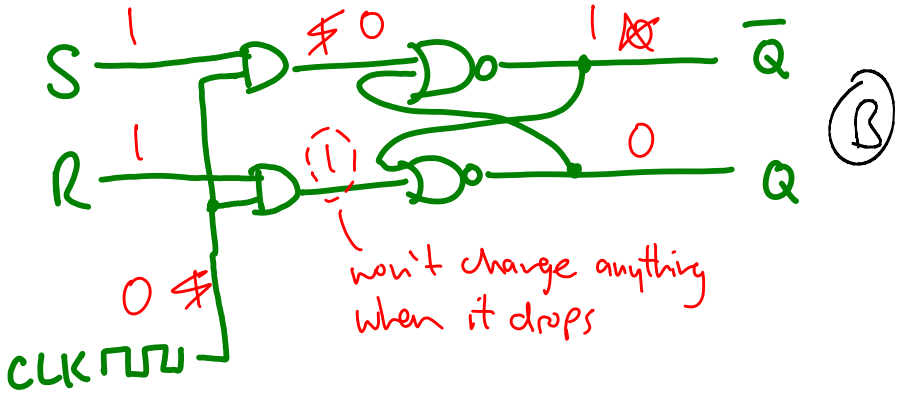
This situation, <u>without a clock</u>, is perfectly stable and well-defined. But problems arise when we add a clock. To keep things simple, assume a level-triggered circuit, in which the inputs are ANDed with the clock signal:



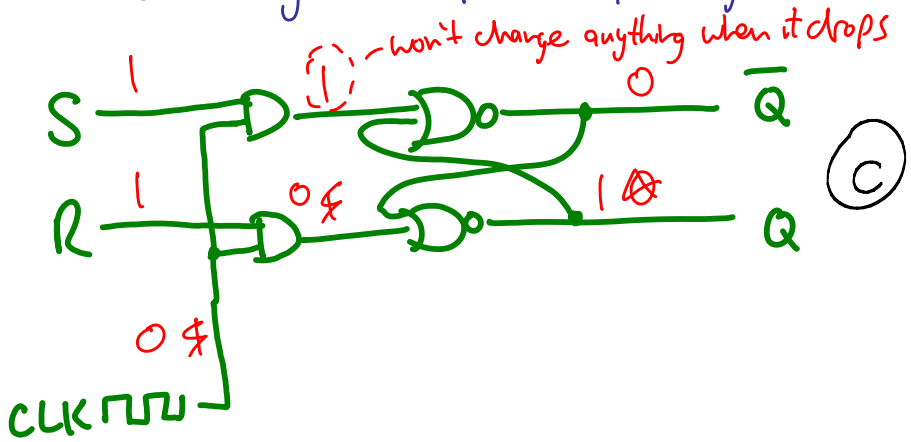
When the clock signal is 1, the situation is essentially identical to situation (A) above:



But when the clock flips to 0, what happens? The output of both AND gates drops to 0, but in reality one will drop very slightly before the other. If the top gate drops first, we get:



But if the bottom gate drops first, we get:



In other words, at the end of the clock cycle, we have no way of knowing whether the circuit is in state (B) or (C). This is what we mean by saying that $Q(t+1)$ is undefined when $S = R = 1$.