1. Virtual memory without TLB

[assume memory is byte-addressable]

logical address format:

page	offset
3 bits	4 bits

physical address format:

frame	offset
2 bits	4 bits

page size = _____

number of pages = _____

number of frames = _____

size of virtual memory (i.e. address space) = _____

size of physical memory = _____

memory references:

cycle	(virtual) address referenced	page fault?	physical address
0	0010100		
1	0010101		
2	1111001		
3	0101100		
4	1110110		
5	1100101		
6	0110110		
7	1010100		
8	1011110		

page table contents:

page	frame	valid
0		0
1		0
2		0
3		0
4		0
5		0
6		0
7		0

main memory contents: (evict using LRU)

frame	data
0	
1	
2	
3	

2. Virtual memory with TLB

[assume memory is byte-addressable]

logical address format:

page	offset
3 bits	4 bits

physical address format:

frame	offset
2 bits	4 bits

page size = _____

number of pages = _____

number of frames = _____

size of virtual memory (i.e. address space) = _____

size of physical memory = _____

memory references:

cycle	(virtual) address referenced	TLB miss or hit?	page fault?	physical address
0	0010100			
1	0010101			
2	1111001			
3	0101100			
4	1110110			
5	1100101			
6	0110110			
7	1010100			
8	1011110			

TLB contents (assume fully associative; evict using LRU):

page	frame

page table contents:

page	frame	valid
0		0
1		0
2		0
3		0
4		0
5		0
6		0
7		0

main memory contents: (evict using LRU)

frame	data
0	
1	
2	
3	